INTEGRATED GIGABIT LOGIC -- STATE OF THE ART ASSESSMENT AND PERFORMANCE PROJECTIONS

Lutz J. Micheel, Gordon G. Rabanus
Air Force Avionics Laboratory
AFAL/DHE
Wright-Patterson Air Force Base, Ohio

ABSTRACT

After an overview of a wide range of technologies featuring sub-nanosecond ring oscillator stage delays, a simple method is described to convert such data into gate delays and flipflop clock rates in larger monolithic integrated circuits. Performance and chip complexity advancement for 1980 and 1985 are projected.

Introduction

The state of the art for conventional kilo and megabit/sec digital IC systems' applications is routinely being covered in a lucid and useful way by the top trade magazines and technical journals[1]. But when the Digital Systems' Designer endeavours to read, say, the latest ISSCC or IEDM proceedings to find out what the future holds in the elusive Gigabit Logic regime, he'll find a bewildering multitude of technologies, all heralding "subnanosecond propagation delays" -- derived from ring oscillators with a fan-in and fan-out of one. Such data is suitable only to prove the feasibility of a new technology and to evaluate device performance; the Systems' Designer needs flipflop clock rates and average gate array propagation delays, with a useful fan-in and fan-out of 2 to 4. The question is, how can we convert ring oscillator data into flipflop clock rates? More importantly, which of these technologies have a reasonable chance to be developed to the point of becoming available for gigabit systems use?

The objective of this paper is, therefore, to shed some light on these questions by offering a simple conversion method that's suitably accurate for MOSFET, MESFET, and other logic types and then to apply this method to published ring oscillator data as an aid in projecting monolithic IC performance and complexities for 1980 and 1985.

State of the Art Overview

First, we should list the more prominent IC achievements of the past year or two that are considered to be contenders for Gigabit Logic, see Table 1. We'll concentrate on general logic circuits suitable for MSI and LSI as distinct from analog-to-digital converters, digital modulators, memories, etc. Most of the published data for the emerging technologies have been derived from Ring Oscillators (RO), with fan-in (FI) and fan-out (FO) of one, which were designed for maximum layout density. The employed minimum design rules are given in parentheses and in each category only the fastest implementation is listed, as a rule. A few VLSI technologies are also added which should eventually prove suitable for subnanosecond gate arrays (see also Table 3 below).

The range of technologies is indeed amazing: Silicon and GaAs are both well represented and the device types include enhancement/depletion MOSFETs, MESFETs, JFETs, and also two bipolar technologies. However, there is no guidance that can be derived from this table in regard to systems' suitability of the very different technologies and circuit concepts proposed.

TABLE 1

CASE	LOGIC FAMILY	TEST VEHICLE	t_{pd}
1	MESFET(0.5μ)[2] GaAs	INVERTER	23ps
2	MESFET(0.5μ)[2] GaAs	RO 5 stages	33ps
3	MOS(0.25μ)[3] Si n-channel	RO 61 stages	64ps
4	MOS(0.5μ)[4] Si punch-thru	RO 13 stages	75ps
5	MESFET(1μ)[5] GaAs FI=3 FO=2	Gate RO 5 stages	83ps(typ)
6	EEIC(0.4μ,eff)[6] Si EF logic	RO 15 stages	85ps
7	SGFL(1μ)[7] GaAs DTL	RO 7 stages	100ps(typ)
8	MOS(0.5μ)[3] same tech. as #3	RO 61 stages	100ps
9	MESFET(1μ)[5] GaAs FI=4 FO=2	Gate RO 5 stages	105ps(avg)
10	MOS(1μ)[3] same tech. as #3	RO 61 stages	125ps
11	EEIC(0.4μ,eff)[6] same tech. as #6	LSI 180 gates	260ps
12	OAT(∿1μ)[8] Si ox. aligned	FF 1.72 GHz	350ps(est)
13	MESFET(1.2μ)[9] GaAs enh. mode	RO 13 stages	280ps
14	ECL (2.5μ, est)[10] Si ox. isol.	LSI ≤700 gate functions	350ps,eff
15	JFET(3μ)[11] GaAs enh. mode	RO 9 stages	1000ps
16	HMOS(2μ)[1,14] Si n-channel	MEMORY 64 kbit	N/A
17	HMOS(∿2μ)[1,15] Si n-channel	MEMORY 64 kbit	N/A
18	VMOS(1.5μ)[1,16] Si V-groove	MEMORY 64 kbit proposed	N/A

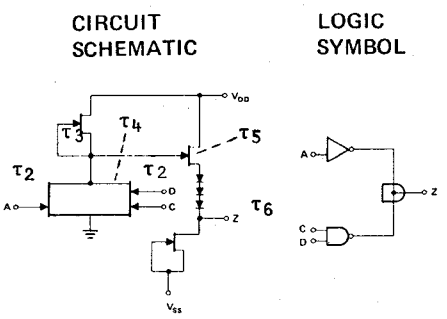
Conversion of Ring Oscillator Data to Flipflop Clock Frequency

The System Designer needs logic gate propagation delay and flipflop clock frequency data derived under realistic load conditions, not highly optimistic ring oscillator stage delays that are really only meant to convey the notion of "feasibility". Most flipflop designs of the delay (D), trigger or toggle (T), and set-reset (RS) type, not just simple latches[12], have an equivalent gate count of 8 to 12; for example, the T-flipflop of the most mature GaAs MESFET logic family is composed of 12 2-input NAND and Wired-OR functions which is equivalent to about 8 3-input OR/NOR gates[5].

On the other hand, the typical RO stage, a simple inverter, should only be considered the equivalent of 1/3 to at most 1/2 of a 3-input OR/NOR gate.

Fortunately, there are measurements of realistically loaded, multiple fan-in ROs as well as flipflops of the mentioned MESFET logic and we'll use them to great advantage. The constituent, "sub-circuit" time constants of these gates are known from measurements on 500μm wide single MESFETs and on gates with 100μm FETs in IC gates.[13] Because the MESFET RO experiments, cases 5 and 9 in Table 1, were executed with FI=1 to 4 and FO=2, their known sub-circuit time constants as shown in Fig. 1 can be used (Step 1 below) to calculate and/or estimate the other time constants (Step 2). Next one must eliminate the second switch transistor and reduce the fan-out to one (Step 3). Then the transition from "normal layout" to the "super-dense RO layout" is to be made (Step 4) in order to arrive at a propagation delay that's comparable to those of cases 3, 4, 6-8, 10, 13 and 15. Van Tuyl estimates a 25% propagation delay improvement for layout optimization[17] which in effect is the same as the Step 4 procedure.-- The dual-gate MESFET has in common with the series-connected MOSFET that it exhibits at low supply voltages a significantly larger t_{pd} than the single-gate MESFET;[5] or the single MOSFET.[pd] Step 5 accounts for this additional delay and we now have an overall gate fan-in of four; in fact, the standard MESFET circuit performs three 2-input functions, (NAND, NAND)Wired-OR, and that's more "logic power" than a 4-input NAND.-- Finally (in Step 6) one arrives at the more useful fan-out =3 by adding 20ps delay based on the load factor of +20%/load, or +15ps/load for the simple gate[13].

FIGURE 1
τ_1 = intrinsic delay or "internal transit time"= 10ps



τ_2 = time constant of 20μm wide drain ∿ 12ps
τ_3 = time constant of 10μm wide load source ∿ 6ps
τ_4 = t. const. of additional metal connecting FET "A" with FET "CD", 115μm^2, ∿ 4ps
τ_5 = output source follower time constant ∿ 9ps
τ_6 = load factor for one load = 15ps

STEP 1
Propagation Delay of full circuit = 83ps
$t_{pd}(A,CD) = 83ps - \tau_5 - 2\tau_6 = 44ps$

STEP 2
$2\tau_2 + \tau_3 + \tau_4 = 44ps - \tau_1 = 34ps$
$\tau_2 = 2\tau_3$ ∴ τ_2∿12ps, τ_3∿6ps, τ_4∿4ps @ 0.038fF/μm^2

STEP 3
$t_{pd}(A) = \tau_1 + \tau_2 + \tau_3 + \tau_5 + \tau_6 \cong 52ps$

STEP 4
$0.8t_{pd}(A) \cong t_{pd}$ of "super-dense" INVERTER ≅ 42ps

STEP 5
Both $t_{pd}(A,CD)=83ps$ and $t_{pd}(CD,CD)=((102+108)/2)ps = 105ps$ were measured[5] and therefore $t_{pd}(CD,CD) \cong 1.25t_{pd}(A,CD)$

STEP 6
With a load factor of +20%/load for ICs covering a larger area than the simple gate (e.g. flipflop's) $t_{pd}(CD,CD,FO=3) = 1.2t_{pd}(CD,CD,FO=2)$

In Table 2 this simple, pocket calculator-type procedure is applied to several of the RO cases of Table 1, primarily in order to derive useful estimates on the *relative* merits of the disparate technologies that appear to be candidates for Gigabit Logic. Of course, the confidence level of these estimates drops significantly when one departs from the MESFET and MOSFET logic families to DTL, ECL, NTL (non-threshold logic, cases 6 and 11 in Table 1), etc.

TABLE 2

LEGEND: * = measured value, d = super-dense layout

LOGIC FAMILY	FI	FO	t_{pd} RO (ps)	t_{pd} Log. (ps)	FF Clock (ps)	FF Clock (GHz)	NOTES
MES(1μ)	3	2		*83			typ
Step 1-3:	1	1	52				
Step 4:	1	1d	42				
Step 5:	4	2		*105	252	*4.0	typ
Step 6:	4	3		125	300	3.3	typ
MES(.5μ)	1	1d	24	*23			
	1	1	*30				
	1	2		36			
	3-4	2		58	139	7.2	
	3-4	3		69	166	6.0	
MOS(.25μ)	1	1d	*64				
	3-4	2		154	369	2.7	
	3-4	3		185	444	2.3	
MOS(.5μ)	1	1d	*100				
	3-4	2		240	576	1.7	
	3-4	3		288	691	1.4	
MOS(1μ)	1	1d	*125				
	3-4	2		300	720	1.4	
	3-4	3		360	864	1.2	
NTL(.5μ)	1	1d	*102				low
	3-4	2		245	588	1.7	pwr
in LSI(avg)	3-4	2-3		*260	624	1.6	gates
	3-4	3		294	706	1.4	
OAT(1μ)	∿2	∿2		280	588	*1.7	
	1	1d	∿83				eff

Technology Assessment for 1980

In Fig. 2 a few prominent subnanosecond IC achievements of 1976-78 are given in a plot of corrected propagation delay (FI=2..4, FO=2..3) versus equivalent gate count (see Definitions below). Then the expected improvements are presented in three ways: (1) Increased complexity only, with minor cell layout and circuit improvements -- some decrease in speed due to larger average connection line lengths, (2) Simultaneous device/circuit improvements and increased complexity -- more or less the same speed, and (3) Drastic technology advancement such as "design rule" improvement from 3μ to 1μ -- large increase of both speed and density. Case (1) results in a slightly upward slanted arrow pointing towards higher IC complexity, case (2) appears horizontal in Fig. 2 and the case (3) arrow points towards significantly reduced gate delays.

The somewhat conspicuous fact that in Table 1 no gate power dissipations were given, now finds an explanation: gate power, in conjunction with layout density and fabrication defect-density, is a limiting factor in the maximum IC chip size that's economically attractive.

Technology Projections for 1985

In Fig. 2 also the apparent trends for the development of Gigabit Monolithic IC Logic are projected up to the mid 1980's period, with all due caution that these are only estimates, even though conservative ones. The information conveyed by Fig. 2 is complemented by Table 3; five clock frequency/propagation delay regimes are used as a convenient means of grouping the various Gigabit Logic IC Families, four of which are being considered in this paper (Regions 2-5). The term "MOS" includes n-MOS, CMOS, CMOS/SOS, etc. (except in Region 5b); e/d = enhancement and/or depletion mode MESFET or JFET. The most promising technologies for Gigabit MSI and LSI are marked with a star.

DEFINITIONS

MESFET, MES: Metal-Semiconductor FET, mostly GaAs; also "Schottky Gate FET"

Equivalent Gate Count: The number of 3-input OR/NOR gates required to duplicate the given logic function

FIGURE 2

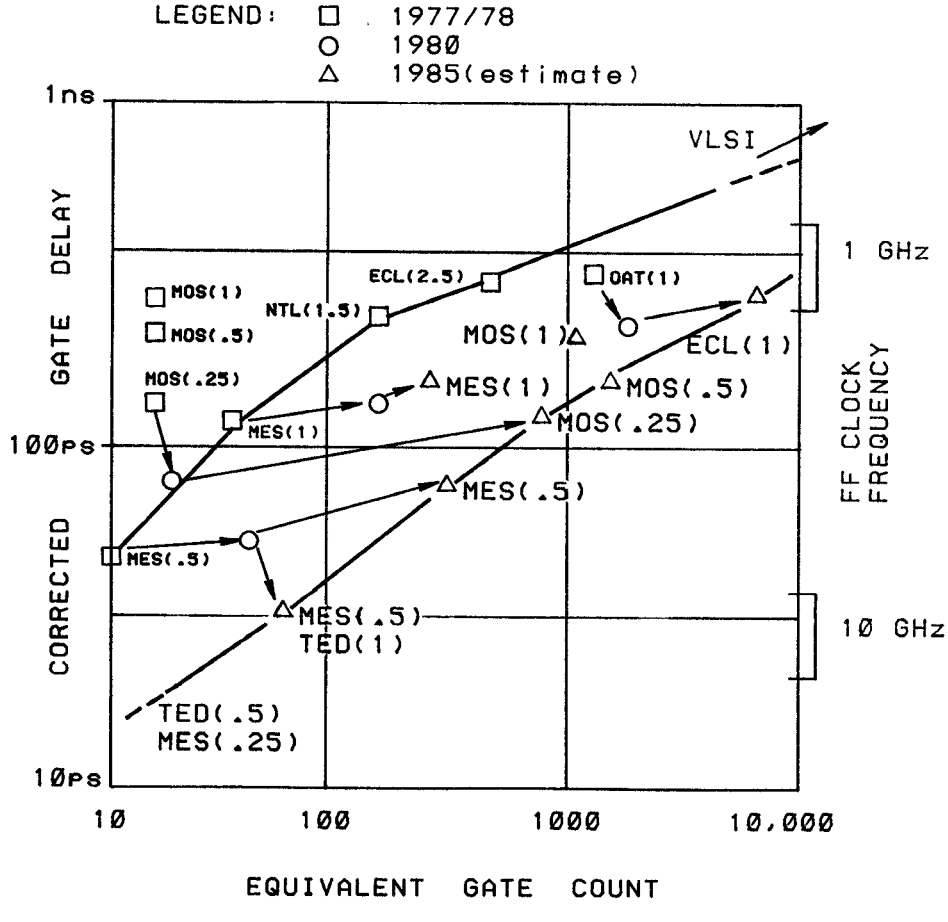


TABLE 3

REGION 1: ≥ 10 GHz Clock Frequency

(a) TED(≤0.5μ) and MESFET(0.25μ): if feasible
(b)*TED(1μ) near 10 GHz for which designs exist

REGION 2: 4-10 GHz

(a)*MESFET(0.5μ), TED(1μ)
(b) TED(2-3μ) near 4 GHz

REGION 3: 2-4 GHz

(a)*OAT(1μ eff), MESFET(1μ), NTL(1μ)
(b) MOS(0.25μ): if feasible
(c)*MESFET(0.5μ) in LSI >300 gate count

REGION 4: 1-2 GHz

(a)*MOS(0.5μ), NTL(1.5μ), ECL(1μ), e-JFET(1μ)
(b) Punch-thru e/d-MOS(0.5μ), e-MESFET(1μ)
(c)*MOS(1μ) near 1 GHz

REGION 5: 0.5-1 GHz, but possibly ≥ 1 GHz

(a)*3D(0.5μ), ECL(2μ), e-JFET(2μ)
(b)*HMOS(2μ), *CMOS/SOS(2μ), *VMOS(1.5μ, eff), CMOS(2μ), *DMOS(<2μ)

CONCLUSIONS

From Fig. 2 and Table 3 we may conclude that quite a few Gigabit IC Technologies will come to fore by 1985; commercial interests and especially the military needs will decide which ones will finally be chosen to be developed to full maturity, i.e., "MSI" and, in some cases, "LSI".

It is quite apparent that several of the areas addressed in this paper deserve much more detailed treatment, in particular the suitability of the various technologies for the wide range of possible systems' applications. This remains a task for future discussions, such as the Tuesday evening Panel Session at this conference, "Applications of High-Speed ICs to Microwave Systems".

REFERENCES

1. Electronics, 18 Aug 1977, p. 91-112, "VLSI Technologies; HMOS, VMOS, DMOS, CMOS/SOS, I^2L."
2. P. Greiling et al, "Electron-Beam Fabricated GaAs FET Inverter," Device Research Conf., June 1978.
3. M. Elliott et al, "Size Effects in e-Beam Fabricated MOS Devices," Int. Electron Devices Meetg., Dec 1977.
4. T. Nakamura et al, "Punch-Through MOSFET for High Speed Logic," ISSCC, Febr. 1978.
5. R. Van Tuyl, Ch. Liechti et al, *"GaAs Digital ICs,"* Government Report AFAL-TR-76-264, Contract F33615-73-C-1242- DDC Accession No. B-018865, April 1977;
   R. Van Tuyl, Ch. Liechti et al, "4 GHz Frequency Division with GaAs MESFET ICs," ISSCC 1977;
   R. Van Tuyl, Ch. Liechti, "GaAs Spawns Speed," IEEE Spectrum, March 1977.
6. T. Sakai et al, "A 100ps Bipolar Logic," ISSCC 1977, p. 196 (also Fig 3, p. 162)
7. R. Eden et al, "Low Power GaAs Dig ICs using Schottky Diode-FET Logic," ISSCC 1978.
8. D. Breuer, *"Gigabit Logic Design,"* Government Report AFAL-TR-76-181, Contract F33615-73-C-1110, April 1977.
9. H. Ishikawa et al, "Normally-Off Type GaAs MESFET for Low Power, High Speed Logic Circuits," ISSCC 1977.
10. W. Braeckelmann et al, "A Masterslice LSI for Subnanosecond Random Logic," ISSCC 1977.
11. R. Zuleeg et al, "Femto-Joule High-Speed Planar GaAs e-JFET Logic," submitted Feb 1978 to IEEE Transactions--ED, special issue on Microwave Semiconductor Devices;
    R. Zuleeg et al, *"Enhancement Mode GaAs JFET MSIC Technol.,"* Government Report AFAL-TR-78-25, Interim Report I, Contract F33615-76-C-1127, Jan 1978.
12. G. Maley, J. Earle, *"The Logic Design of Transistor Dig. Computers,"* Prentice-Hall 1963;
    M. Phister, *"Logical Design of Dig. Computers,"* J. Wiley and Sons, 1958.
13. R. Van Tuyl, Ch. Liechti, "High-Speed Integrated Logic with GaAs MESFETs," IEEE Journal--SC, Oct 74; also ISSCC 1974.
14. H. Yoshimure et al, "A 64Kbit MOS RAM," ISSCC 1978.
15. D. Wilson et al, "A 100ns 150mW 64Kbit ROM," ISSCC 1978.
16. K. Hoffmann et al, "VMOS Dynamic RAM," ISSCC 1978.
17. R. Van Tuyl, Ch. Liechti, "High-Speed GaAs MSI," ISSCC 1976.
18. B. Bosch, "Gigabit Electronics," European Microwave Conference, Sept 1977; also Proceedings IEEE, to be published 1978.